ABSTRACT OF THE DISCLOSURE

A folded common cascode circuit with symmetric parallel signal paths from the differential inputs to a single ended output provides a low skew, low jitter, low power, high speed differential in/out amplifier. There is a differential input stage followed by a load or current summation stage with all gates tied together, and then a second differential stage. The dynamic voltage range of the second stage allows for lower Vcc operation while providing improved jitter operation. The signal paths on either side of the differential amplifier are made equal with equal loads along each path. Pairs of complementary NMOS and PMOS transistor pairs with parallel complementary biasing current mirroring stacks on the cascode circuitry have all their gates connected together. The layout maintains symmetrical parallel signal paths and symmetrical amplification and impedance loading from differential input to the differential output. Output inverters provide a higher drive capability.